Modeling of Passive Elements with ASITIC

Ali M. Niknejad

University of California, Berkeley, CA 94720-1770, USA

Abstract — **Passive elements are key building blocks in realizing fully integrated low cost RF transceivers. The analysis and modeling of passive elements is critical in the design and optimization of building blocks, especially when the quality of passive elements determines the overall achievable performance. Analysis of passive elements near the silicon substrate, though, necessitates solving Maxwell's equations. Furthermore, simulation of passive elements in tools such as SPICE requires lumped-element equivalent circuit models derived through optimization. ASITIC is a software tool that aids the RF designer in the process of design and simulation of such structures.**

I. Introduction

Passive elements constructed on the silicon substrate couple strongly to the conductive substrate resulting in excess energy loss and a resulting decrease in the quality factor of such devices. Furthermore, the metal layers of a typical IC process are sufficiently wide and potentially sufficiently thick that current distribution is non-uniform in the metal layers at microwave frequencies. Metal layers can be put in very close proximity to one another due to the fine lithographic dimensions of the IC process and thus current distributions in a given conductor are often strongly influenced by nearby conductors. These effects require the solution to partial differential equations (PDE) derived from Maxwell's equations in order to fully account for the high-frequency energy storage and loss mechanisms.

The full-wave solution of Maxwell's equations, though, is computationally expensive and time-consuming. Often a quasi-static solution to Maxwell's equations is sufficiently accurate to characterize the physical device. Transmission lines, for instance, satisfy the static field equations in the traverse direction. Furthermore, for the majority of passive elements realized on-chip, the dimensions of the structure are usually much smaller than the wavelength. Thus, time-delay in the mutual coupling from element to element can be neglected and Maxwell's equations simplify to static capacitance and inductance computations. Measurements and simulations have verified this quasi-static assumption.

ASITIC [1], *A*nalysis and *S*imulation of *I*nductors and *T*ransformers for *I*ntegrated *C*ircuits, first described in [2][3], is a tool for the analysis of passive elements fabricated on the Si substrate. Maxwell's equations are solved under the quasi-static assumption and a modified Partial Element Equivalent Circuit (PEEC) [4] technique is used to derive n-port parameters for the device. Under the appropriate conditions, ASITIC simulations are very fast and accurate. This paper will discuss these required conditions by first describing how the tool works and next through several practical examples.

II. Passive analysis and modeling problem

Devices fabricated in a standard IC process consist of a geometric structure residing on the metal and polysilicon layers, with connections to the substrate or well in the form of contacts, rings, or patterns. Given the layout of the device and the relevant process data such as the conductivity, permittivity, permeability, loss tangent, and thickness of the layers, electromagnetic analysis of the device is performed to obtain n-port matrix parameters. This is often performed in the frequency domain and constitutes the most time-consuming portion of the problem. In a design problem, the layout is modified and the analysis is repeated until given electrical specifications are met.

While the frequency-dependent matrix parameters can be used directly in linear and time-harmonic analysis, an equivalent lumped circuit representation is necessary to analyze the devices in conjunction with other non-linear devices in SPICE. Simple lumped element circuit models are often insightful in the design of the circuitry and therefore circuit designers prefer them to a black-box approach to modeling. Optimization is used to minimize the difference between the n-port parameters derived from EM analysis and the n-port parameters of the lumped model equivalent circuit. It is desirable to obtain a match over a wide frequency range, including DC to establish the circuit operating point. In RF circuits, a match at the fundamental and several harmonics is desired.

II. Asitic overview

A block diagram of ASITIC appears in Fig. 1. The user interface is both textual and graphical. ASITIC can

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generate several commonly used structures such as spiral inductors, multi-metal inductors, transformers, and center-tapped differential inductors. Scripting capabilities can be used to extend the geometric generation process. The graphical representation of the structures is represented in 2D using the standard X11 libraries and 3D using the OpenGL library.

Internally ASITIC uses rectangular meshing to represent arbitrary geometric structures as composites of simpler rectangular blocks with non-constant charge and current density. For the capacitance matrix calculation ASITIC further confines the rectangles to lie on a Manhattan grid pattern to facilitate analysis with a 2D FFT.

The back-end of ASITIC relies on efficient numerical libraries such as LAPACK [5] and QUADPACK [6] to perform matrix inverse computations and numerical integral evaluations. LAPACK in turn relies on an efficient implementation of basic linear algebra subroutines (BLAS) to facilitate the computations. ATLAS [7] is used to automatically generate such a library. Fast FFT computations are also needed, but fortunately the data generated by the FFT can be saved to secondary storage and re-used in later computations

A. Capacitance Matrix Computation

The capacitance meshing engine further sub-divides each block or segment into many sub-elements or panels of constant charge density. The voltage on a panel is also assumed to be constant. For a typical spiral inductor, for instance, several hundred panels are sufficient to compute the capacitance matrix for the segment-to-segment interactions. Poisson's equation may be written as

$$\nabla^2\phi = -\left(\frac{\rho_{\text{metal}}}{\varepsilon} + \frac{\rho_{\text{substrate}}}{\varepsilon}\right) \quad (1)$$

where due to the conductive nature of the substrate, charges in the substrate are shown explicitly in the above equation. The substrate has a significant influence on the capacitance and the loss. At each frequency of interest, each segment-to-segment coupling term can be represented as a capacitor in series with a resistor. To compute this lossy capacitance matrix, the following modified Poisson's equation is solved where each substrate layer is modeled as an equivalent lossy dielectric

$$\nabla^2\phi = -\frac{\rho}{\varepsilon + j\sigma/\omega} \quad (2)$$

To avoid meshing the substrate a Green function approach is used to characterize the response of the substrate to an impulse function of charge. The convolution of this impulse response and the actual charge distribution on the metal layers can be used to obtain the potential.

This approach was first applied to the substrate coupling problem in [8] and layer extended to the passive analysis problem in [9]. It should be noted that the Green function formulation is also a candidate for multi-pole expansion [10] and with an increase in computational efficiency for solving very large problems.

B. Partial Inductance Matrix Computation

The Grover-Greenhouse method of computing the inductance of passive elements is in widespread use. Analytical expressions for common geometric arrangements have been tabulated. These formulas give the sum of the internal and external inductance strictly valid at DC where the current distribution in the body of conductors is assumed uniform. While the internal inductance accounts for only a small fraction of the total inductance, the internal resistance increases rapidly due to eddy currents in the metallization. This phenomenon is better known as skin effect. To capture skin and proximity effects, ASITIC sub-divides each segment into filaments of constant current and computes the partial inductance matrix for this family of filaments. The filaments are grouped by enforcing charge conservation and by neglect of displacement current in the body of the conductors. This procedure is first described in [11] and a more efficient approximation is described in [2].

The time-varying magnetic fields penetrating the substrate produce solenoidal electric fields in the substrate that give rise to bulk eddy currents. These currents in turn give rise to an induced time-varying magnetic field in opposition to the fields generated by the passive device. More importantly, the eddy currents give rise to a loss mechanism. Conceptually, one can view this loss in analogy with a transformer where the primary represents the passive device and the secondary represents the substrate. Since the substrate is terminated by its own resistivity, power loss occurs through the secondary. This viewpoint is especially fruitful in understanding the corresponding loss in inductance seen by the primary. For an infinitely conductive substrate, for instance, the inductance value is reduced to

$$L_{\text{eff}} = L_p + M(I_s/I_p) = L_p(1-k^2) \quad (3)$$

whereas for an insulating substrate the inductance and loss are unaltered since I_s is zero. To include the response of the substrate the following partial differential equation must be solved to obtain the inductance matrix

$$\nabla^2 A = -\mu J + j\omega\mu\sigma A \qquad (4)$$

where the first term on the right hand represents the current in the metallization and the second term represents the eddy currents. In [12] it is shown that the Grover/Greenhouse technique is tantamount to solving (4) in two dimensions with filamental excitation resulting in a logarithmic Green function. A 2D solution of (4) for common-substrate profiles in carried out in [13] and results in an integral expression for the reflected impedance of a filament due to the substrate. Using these expressions, the inductance matrix can be modified to include the effects of the substrate.

B. Partial Element Equivalent Circuit Formulation

Given the partial inductance and capacitance matrix for a set of conductors, and the electrical interconnection of the various conductors, the *n*-port network parameters are readily derived by enforcing KVL and KCL relations. This technique is equivalent to solving Maxwell's equations [4] when we neglect time delay. For instance, for a series interconnection of segments we obtain

$$i_k - i_{k+1} = \sum_j Y^C_{k,j} \tfrac{1}{2}(v_j + v_{j+1}) \qquad (5)$$

$$v_k - v_{k+1} = \sum_j Z^M_{k,j} \tfrac{1}{2}(i_j + i_{j+1}) \qquad (6)$$

where the voltage and currents in each segment are v_k and i_k and the impedance and admittance matrix Z^M and Y^C are computed as described.

III. EXAMPLES

A. Spiral Inductors

Integrated inductors are usually realized as spiral coils. In typical applications a particular value of inductance is desired with maximum quality factor realized in a given area of silicon. To minimize the resistance or to maximize the inductance in a fixed area, multiple spirals on different IC metal layers can be realized and connected in shunt or series. Additionally, tapering of the inner turns of the spiral can enhance the Q factor since inner turns are impinged by a stronger magnetic field than outer turns.

Consider a 9 nH square spiral fabricated over a conductive substrate where in Fig. X the measured *s*-parameters are compared to simulated parameters. It is important to note that the process parameters used in the simulation are not tweaked to match the measurements. Good correspondence is observed over a wide frequency range of .1 GHz – 14 GHz with ASITIC predicting a self-resonant frequency of 4.15 GHz whereas the measured resonance frequency is observed at 4.25 GHz.

The simulated and measured quality factors are shown in Fig. Y. Note that after resonance the quality factor is negative as the device acts like a capacitor and again a good match is observed between theory and measurement. As shown in the plot, it is critical to model the eddy currents in the substrate to account for the reduced high-frequency quality factor.

To model such structures in SPICE, a compact circuit model such as that shown in Fig. Z [14] can be optimized to fit the data over a wide frequency range. This model contains elements that model skin and proximity effects and thus it more accurately matches physical results.

B. High Frequency Substrate Coupling

The capacitance matrix engine of ASITIC can be used to analyze the electrically induced substrate losses. Substrate coupling between bonding pads, inductors, capacitors, and other metal structures can be readily analyzed with ASITIC. The substrate spreading resistance of varactors and transistors can also be analyzed. For instance, the MOSFET drain and source impedance to the substrate contact can be analyzed with ASITIC. Thin diffusion regions can be modeled by equivalent metal layers placed inside the substrate.

V. CONCLUSION

The analysis and modeling of passive devices have been illustrated using ASITIC. The internal algorithms of ASITIC and the resulting limitations in the operation of the tool have been presented. Several common example structures have been used to illustrate the design process.

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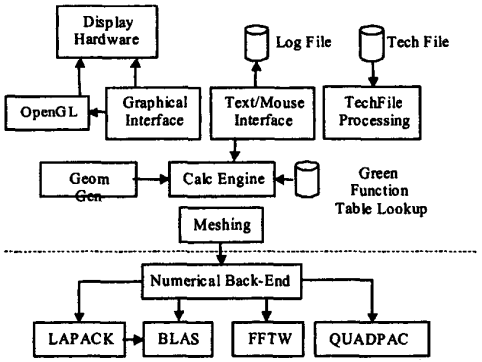

Fig. 1 ASITIC block diagram.

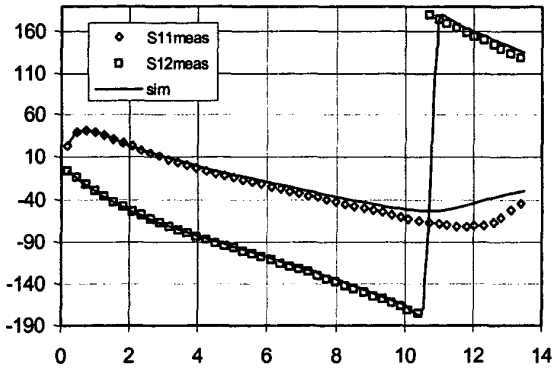

Fig.3 Phase of measured and simulated *s*-parameters.

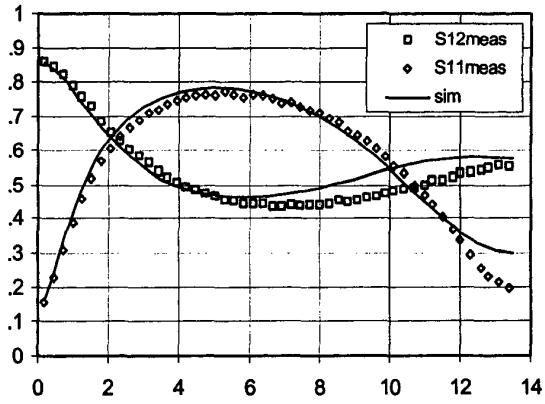

Fig. 2 Magnitude of measured and simulated *s*-parameters.

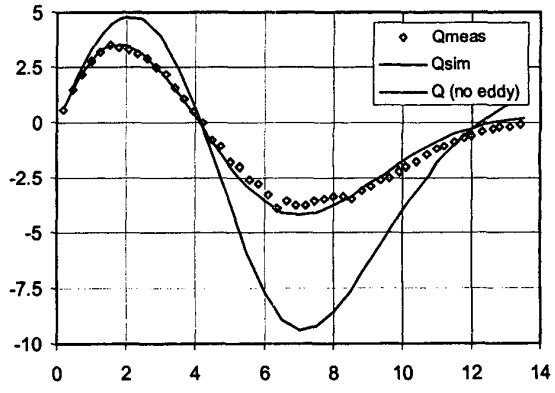

Fig. 4 Measured and simulated quality factor.